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Pulse Width Prediction Control Technique Applied to a Half-Bridge Boost

Técnica de Control de Predicción de Ancho de Pulsos Aplicada a un Boost Medio Puente

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Abstract

The pulse width prediction control technique has been widely used in AC-DC converters with power factor correction in boost topology, where satisfactory results have been reported without the need to use classic control laws. However, this technique has not been explored for other types of ACDC converters with power factor correction. In this work, the use of this technique is proposed in an AC-DC converter with power factor correction in a half-bridge boost topology. This topology presents high efficiency because it uses the least number of semiconductors compared to other topologies. In this technique the duty cycle is predicted by processing the average values of state and input variables of the converter in half bridge boost topology, using only four multiplications and five additions, which implies less complexity in its implementation. For its validation simulations were performed using MATLAB R Simulink, where it was possible to observe values of power factor and THD comparable with other control methods such as non-linear carrier control, and conventional analog control, both reported in the literature.

Keywords: Half-bridge Boost Topology, Power Factor Correction, IEC61000-3-2, Pulse Width Prediction Control.

Resumen

La técnica de control de predicción de ancho de pulsos ha sido ampliamente utilizada en convertidores AC-DC con corrección de factor de potencia en topología boost, donde se han reportado resultados satisfactorios sin necesidad de usar leyes clásicas de control. Sin embargo, ésta técnica no ha sido explorada para otros tipos de convertidores AC-DC con corrección de factor de potencia. En este trabajo, proponemos el uso de ésta técnica en un convertidor AC-DC con corrección de factor de potencia en una topología de boost medio puente. Esta topología presenta una alta eficiencia dado que usa el menor número de semiconductores comparada con otras topologías. En ésta técnica el ciclo de trabajo es predicho al procesar los valores promedio de las variables de entrada y estado del convertidor en topología boost medio puente, usando únicamente cuatro multiplicaciones y cinco adiciones, lo que implica menos complejidad en su implementación. Para su validación, se realizaron simulaciones usando MATLAB R Simulink, donde fue posible observar valores de factor de potencia y THD comprables con otros métodos de control como control de portador no lineal y control convencional análogo, ambos reportados en la literatura.

Palabras clave: Topología de Boost Medio Puente, Corrección de Factor de Potencia, IEC61000-3-2, Control de Predicción de Ancho de Pulsos.

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1. Introduction

Currently, most electronic equipment such as power sources, battery chargers, appliances, communication systems, medical equipment, among others, need a constant DC voltage bus from the AC line. For this they include in the input stage the simplest and most conventional AC-DC converter (SC), which comprises a diode bridge and an electrolytic capacitor with a high capacitance value [1]. The SC is widely used because of its very low cost; however, the waveform that the converter absorbs from the AC line is not sinusoidal and has a high crest factor, due to the small conduction angle used by the electrolytic capacitor to charge [2]. For this reason, the waveform of the line current has a high total harmonic distortion that produces the following disadvantages: first, reduction of the power factor, which implies a decrease in the AC line available power [3]; second, harmonics injection to the line voltage that interfere with other electronic equipment connected to the same line [4]; finally, line voltage instability [5].

Consequently, the SC cannot meet the IEC-61000-3-2 and IEEE Std 519 European and/or American standard respectively. These standards impose the limits on AC current harmonics, as well as in total harmonic distortion of the electronic equipment that is fed by the AC line [6]. In order to meet these standards, different studies in the area of power electronics have focused on improving the power factor of electronic equipment that are connected to the line.

For this purpose, AC-DC converters with power factor correction (CPFC) are the best alternative [7] [8]. Several authors have analyzed the operation of the CPFC topologies, from the most classic such as: boost [9] [10], buck-boost [11], flyback [12] [13] and half bridge boost [14] [15], up to the most recent: no diode bridge [2] [16] [17], interleaved [18] and flyback with dual-purpose inverter [19]. Within these, the AC-DC converters with power factor correction in half bridge boost topology (CPFC-HBB) has the simplest conversion circuit and with fewer switches[20], so the main advantage of the CPFC-HBB is that it presents high efficiency, since at any time there is only a voltage drop, which is produced by the working semiconductor [21]. Another advantage of the CPFC-HBB is to allow its power flow to be bidirectional; this explains why the CPFCHBB is widely used in power factor correction applications [22].

On the other hand, other authors have studied and implemented control methods for the CPFC-HBB such as: conventional analog [7], by replacing a boost diode and inductor with a switch and transformer, respectively [23], current-by hysteresis [14] [24], non-linear Lyapunov technique [25] [26] and non-linear carrier control [27] [28], or current sensor-less control [29].
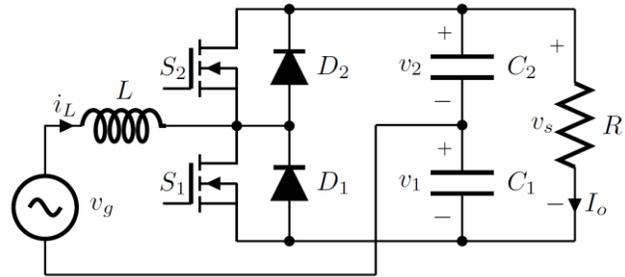
Figure 1 CPFC circuit in half bridge boost topology

The emergence of low-cost microprocessors, digital signal processors (DSP) and programmable gate array (FPGA) has made it possible for new control strategies to emerge, which have advantages such as programmability and lower sensitivity to parameters variation. Some of these control strategies that predict the CPFC duty cycle from the inductance, reference current, input voltage and output voltage reference, have been introduced in previous works [30] [31], nevertheless, these control strategies were implemented in CPFC in boost topology .

In this work, we propose a strategy for predicting the duty cycle for a CPFC-HBB, in order to obtain a high power factor. The aim of this work is to design a control strategy for CPFC-HBB, by means of predicting the duty cycle starting from the average model. This work is divided as follows: in Section 2, a rigorous and detailed analysis of the proposed control strategy is presented using the average circuit model; in section 3, the simulation results of the proposed control that was implemented in MATLAB R Simulink; in section 4, the conclusions and future work.

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2. Predictive Control Strategy for a CPFC-HBB

The CPFC-HBB circuit used with the predictive control strategy is shown in Fig. 1. The CPFC-HBB consists of two switches, in this case MOSFET's (S_1, S_2) each with their respective intrinsic diode, an inductance on the AC side (L), two capacitors on the DC side (C_1, C_2) and a load resistance (R).

The analysis of the proposed control strategy is derived from assuming that all CPFC-HBB circuit components are ideal. To begin with, the inductance voltage equation that is given by:

$$\hat{v_L} = L \frac{d\hat{i_L}}{dt}, \qquad (1)$$

Here $\hat{i}_L$ and $\hat{v}_L$ are the instantaneous current and voltage of the inductance respectively. By solving for $\hat{i}_L$ and integrating from t to $t + T_s$:
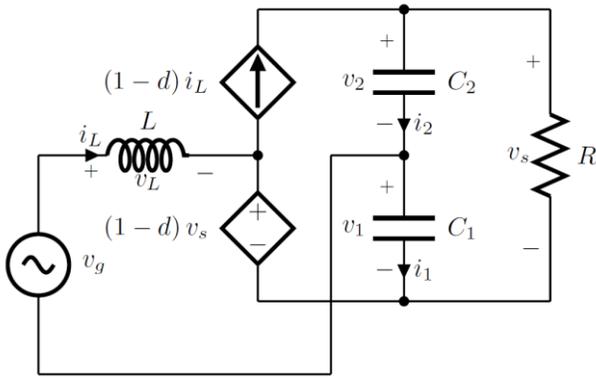
Figure 2 Average circuit model of the CPFC-HBB.

Figure 3 Waveform of the instantaneous and average input current.

$$\hat{i}_L\left(t+T_s\right) - \hat{i}_L\left(t\right) = \frac{1}{L}\int_t^{t+T_s} \hat{v}_L d\tau = \frac{T_s}{L}v_L, \qquad (2)$$

Here $\hat{i}_L(t)$ is the initial current in the inductance and $\hat{i}_L(t+T_s)$ is the desired current at the end of the period to achieve a unit power factor in the CPFC-HBB. In [20] it was determined that the left side of equation 2 is the net change in the inductance current over a switching period, also noting that said change is exactly equal to the switching period for the average slope.

On the other hand, Fig. 2 shows the average circuit model (ACM), in which the switches are replaced by controlled sources [20]. S_1 is replaced by a voltage source whose value is equal $(1 - d)\, v_s$, where d is the duty cycle of S_1 and v_s is the sum of the average voltages of capacitors v_1 and v_2, likewise, S_2 is replaced by a current source with value equal to $(1 - d)\, i_L$, where i_L is the average current of the inductance.

The ACM is used to obtain expressions that define the state equations averaged over one switching period, to determine the steady-state values CPFC-HBB easily and finally, to simulate efficiently the CPFC-HBB, this means that time and memory storage decreases compared to the simulation using the switches. However, the switch model is useful and necessary to determine currents and peak voltages experienced by the CPFC-HBB.

When applying Kirchhoff's law of voltages around the ACM mesh, composed of v_g, L, $(1 - d)\, v_s$ and C_1, we obtain the average voltage of inductance v_L, which is defined by:

$$v_L = v_g + v_1 - (1 - d)\, v_s. \qquad (3)$$

The averaged state variables of the CPFC-HBB are i_L, v_1 and v_2. However, the voltage in the load resistance is vs, for this reason the state variables v_1 and v_2 are changed to the new state variables v_s and v_d, which respectively represent the capacitors voltage sum and voltage difference. The state variable i_L stays the same, then v_s and v_d are defined by:

$$v_s = v_1 + v_2 \qquad (4)$$

$$v_d = v_1 - v_2, \qquad (5)$$

Solving v_1 from equations 4 and 5:

$$v_1 = \frac{v_s}{2} + \frac{v_d}{2}, \qquad (6)$$

By substituting equation 6 in 3:

$$v_L = \frac{2d - 1}{2}v_s + \frac{1}{2}v_d + v_g, \qquad (7)$$

Replacing equation 7 in 2, the duty cycle d is given by:

$$d\left(t\right) = \frac{1}{v_s(t)}\left[\frac{L}{T_s}\hat{i}_L\left(t+T_s\right) - \frac{L}{T_s}\hat{i}_L\left(t\right) + \frac{1}{2}v_s\left(t\right) - \frac{1}{2}v_d\left(t\right) - v_g\left(t\right)\right]. \qquad (8)$$

When observing Fig. 3, it is established that the net change in the inductance current over a switching period can be expressed in terms of the average input current i_L, hence, equation 8 becomes:

$$d\left(t\right) = \frac{1}{v_s(t)}\left[\frac{L}{T_s}i_L\left(t+T_s\right) - \frac{L}{T_s}i_L\left(t\right) + \frac{1}{2}v_s\left(t\right) - \frac{1}{2}v_d\left(t\right) - v_g\left(t\right)\right]. \qquad (9)$$

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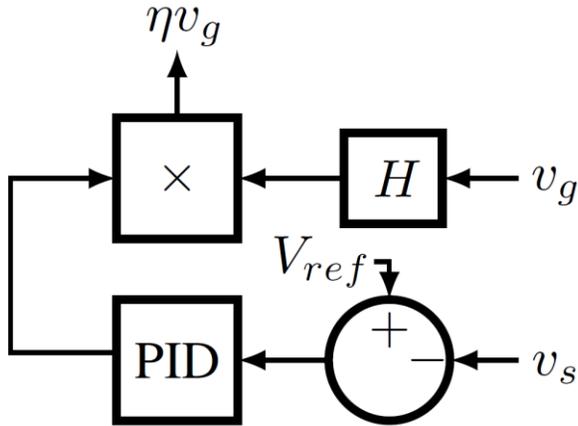
Figure 4 Output voltage control loop diagram.

The value of the duty cycle can be known, as long as all the variables to the right of equation 9 are known. However, the inductor current at the end of the switching period $i_L(t + T_s)$ is unknown. In order to obtain a unit power factor in the CPFC-HBB, the value of this current must be proportional to the input voltage v_g value evaluated in $t + T_s$. Although this voltage is also unknown, it can be replaced by the input voltage v_g evaluated in t, hence, if the switching frequency is much higher than the input voltage frequency, thus, we can say that $v_g(t)$ is a good approximation of $v_g(t + T_s)$, so that equation 9 is changed to:

$$d(t) = \frac{1}{v_s(t)} \left[\eta v_g(t) - \frac{L}{T_s} i_L(t) + \frac{1}{2} v_s(t) - \frac{1}{2} v_d(t) - v_g(t) \right], \quad (10)$$

Here ηv_g is the reference current and η is the peak value of the reference current that governs the output voltage v_s, η is also the product, as shown in Fig. 4, between the output of the PID regulator block that is in the loop that controls v_s and the gain of block H, which serves to take a sample of the input voltage v_g to the multiplier.

We should also mention that the output voltage is controlled to follow the reference voltage V_{ref}, therefore, the output voltage vs becomes a constant value equal to V_{ref} and the division by $v_d(t)$ which is performed in equation 10 is no longer necessary, thus, duty cycle d can be expressed as:

$$d = \frac{1}{V_{ref}} \eta v_g - \frac{L}{V_{ref} T_s} i_L + \frac{1}{2} - \frac{1}{2V_{ref}} v_d - \frac{1}{V_{ref}} v_g, \quad (11)$$

The duty cycle d in equation 11 processes the current average values of the reference current ηv_g, the inductance i_L, the input voltage v_g current and the voltage difference v_d, together with the constant terms mentioned above; likewise, it is shown in equation 11 that only four multiplications and five additions are needed to implement the computation of d.
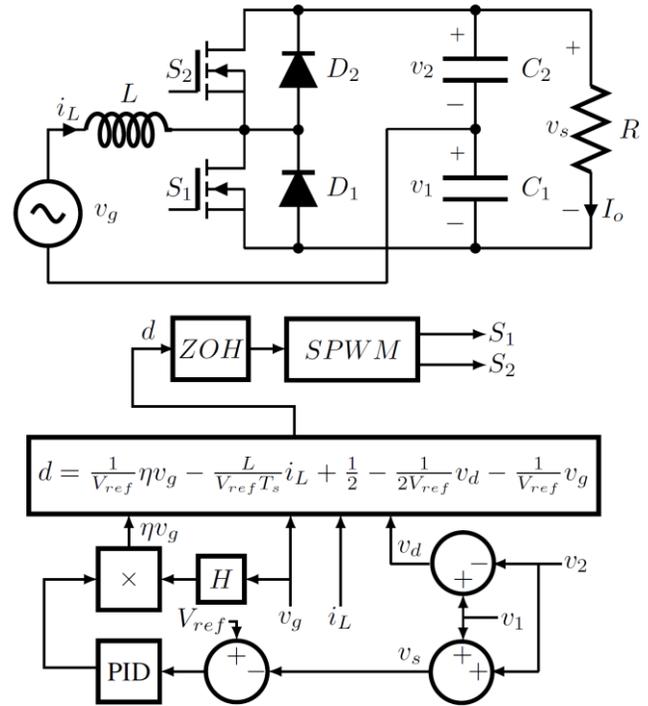
Figure 5 Diagram of the proposed duty cycle control.

The inductance current is controlled by d, so that it follows the reference current, with the purpose that the power factor is unitary. However, in $t + T_s$ the inductance current i_L is not exactly the same, but very close to the reference current ηv_g.

The block diagram of the pulse width prediction control (PWPC) proposed for the CPFC-HBB is shown in Fig. 5. This diagram shows how block d implements the calculation of equation 11, also, it shows that the duty cycle calculated d by that block passes through a *ZOH* zero-order hold before entering the pulse width modulator block *SPWM*, which holds d within a switching period T_s.

With the proposed PWPC, the current inductance i_L of the CPFC-HBB follows the reference current and the output voltage vs of the CPFC-HBB follows the reference voltage. On the other hand, [9] confirmed the existence of the voltage imbalance in the capacitors; they also researched the causes that produced it and provided a control scheme to eliminate it, this scheme consists in adding the difference between v_1 and v_2 to the reference current multiplied by a gain. The PWPC proposed in this work, eliminates the capacitor voltage imbalance, since as can be seen in Fig. 5, it has this control scheme in its block diagram. The work of [9] suggests that the value of the block gain processing the difference between v_1 and v_2 must be less than or equal to 0.1 ωC, being ω the angular frequency of v_g, and C the capacitance value of any of the capacitors, so that the voltage imbalance is zero.
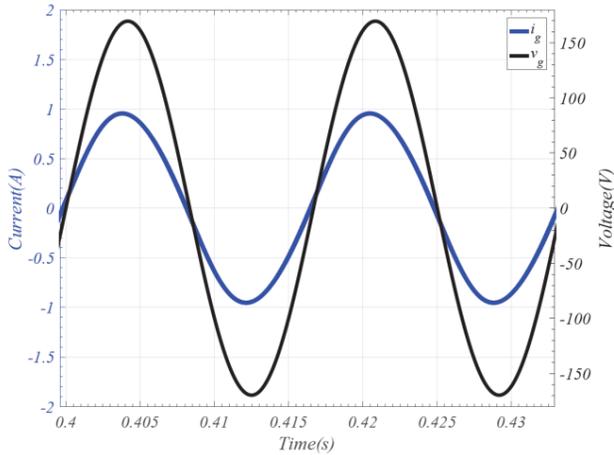
Figure 6 v_g and i_g waveforms; I_o = 200 mA, PF = 0.9954, THD = 2%.
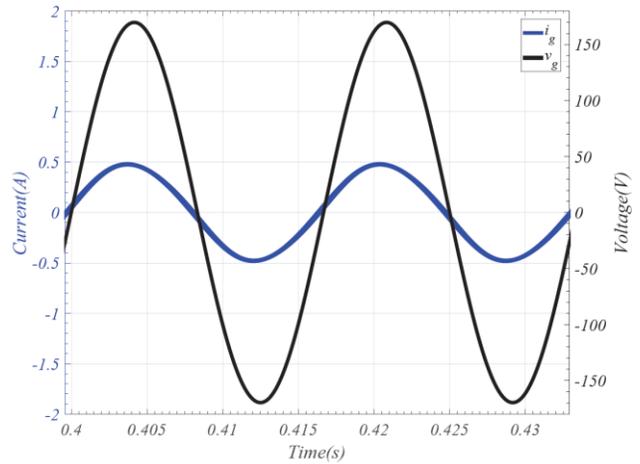
Figure 8 v_g and i_g waveforms; I_o = 100 mA, PF = 0.9913, THD = 3.1%.
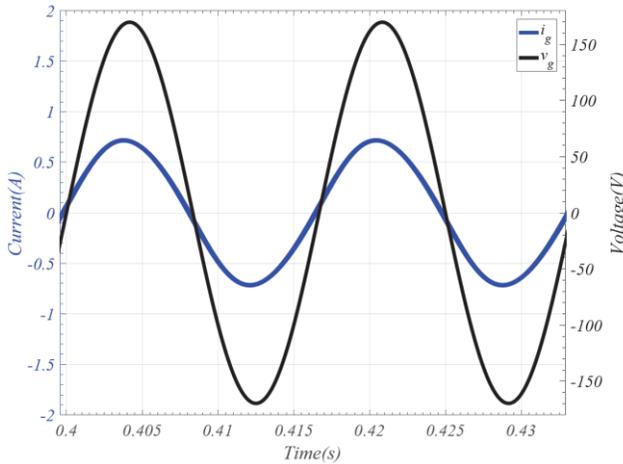
Figure 7 v_g and i_g waveforms; I_o = 150 mA, PF = 0.9941, THD = 2.4%.
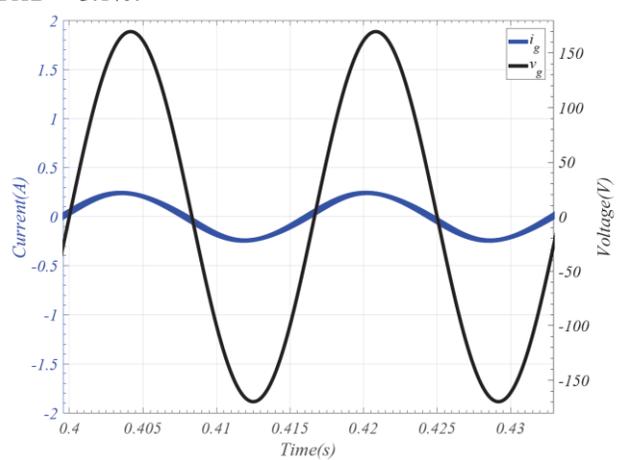
Figure 9 v_g and i_g waveforms; I_o = 50 mA, PF = 0.9796, THD = 5.6%.

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Table 1 Parameter values of the CFPC-HBB.

Circuit parameter	Symbol	Value
Inductance	L	5 mH
Output capacitors	$C = C_1 = C_2$	100 μF
Line frequency	f_l	60 Hz
Switching frequency	f_s	50 kHz
Load resistance	R_L	2 kΩ
Peak line voltage	V_p	170 V
Capacitor voltage	v_1, v_2	200 V

3. Results

A CPFC-HBB with the proposed PWPC strategy was simulated using MATLAB R Simulink, with the circuit parameters that are shown in Table 1, likewise, it was considered that the input voltage is sinusoidal.

The experimental results show that a high power factor is obtained under stationary and transient conditions, these results are shown in subsections 3.1 and 3.2.

3.1 Test results in steady state

Voltage and the input current (v_g and i_g) waveforms of the CPFC-HBB with maximum load current I_o = 200 mA, are shown in Fig. 6.

The power factor (PF) with this load condition is 0.9954 and the total harmonic distortion (THD) is 2%. The waveforms v_g and i_g for I_o = 100 mA, are shown in Fig. 8, the PF with this load condition is 0.9913 and the THD is 3.1 %. The waveforms v_g and i_g for I_o = 50 mA, are shown in Fig. 9, the PF with this load condition is 0.9796 and the THD is 5.6 %. Also, when looking at Figs. 6-9, it can be stated that as the load increases the PF increases, and at the same time, the THD decreases.
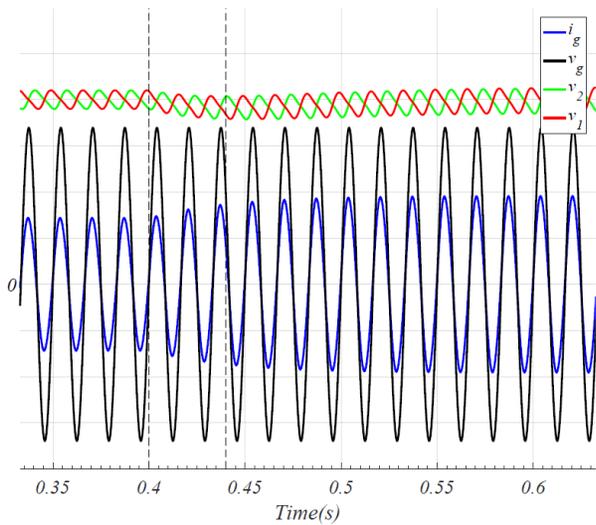
Figure 10 i_g, v_1 and v_2 waveforms in load transient state; I_o changed from 150 mA to 200 mA, v_g = 50 V/div, v_1 and v_2 = 50 V/div, i_g = 1 A/div.
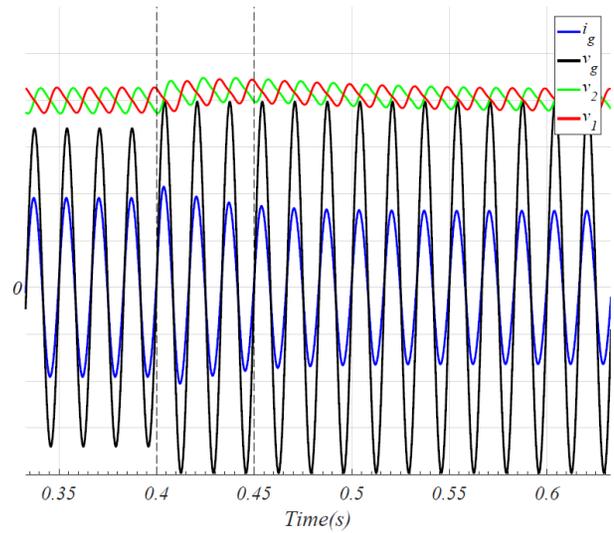
Figure 12 i_g, v_1 and v_2 waveforms for step input voltage change; v_g changed from 120 V to 140 V, v_g = 50 V/div, v_1 and v_2 = 50 V/div, i_g = 1 A/div.
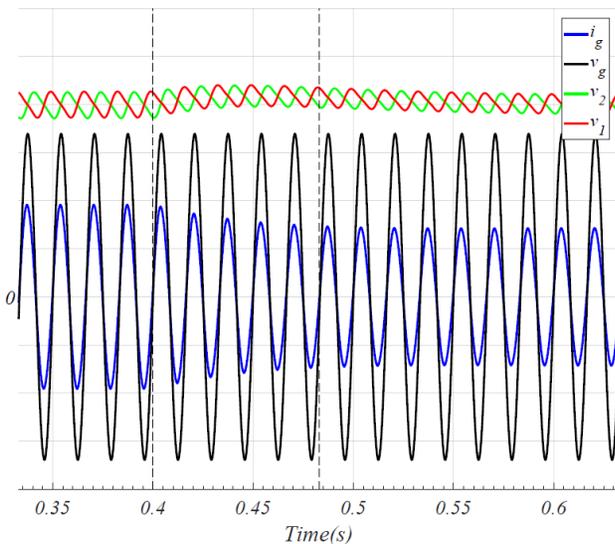
Figure 11 i_g, v_1 and v_2 waveforms in load transient state; I_o changed from 200 mA to 150 mA, v_g = 50 V/div, v_1 and v_2 = 50 V/div, i_g = 1 A/div.
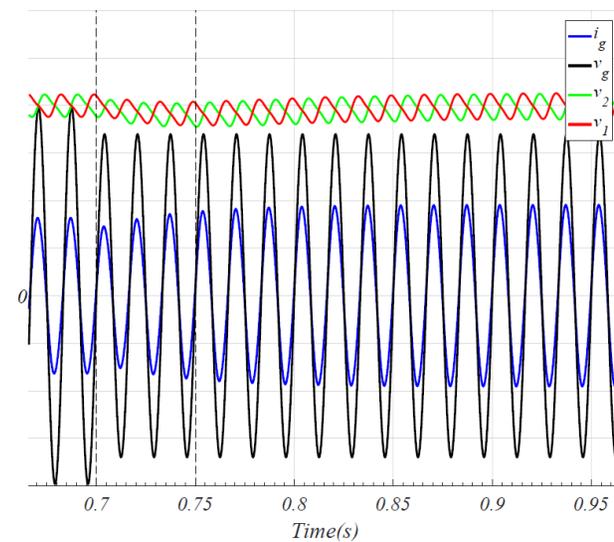
Figure 13 i_g, v_1 and v_2 waveforms for step input voltage change; v_g changed from 140 V to 120 V, v_g = 50 V/div, v_1 and v_2 = 50 V/div, i_g = 1 A/div.

Test results show that the proposed control method for CPFC-HBB, can achieve a near unit power factor and low total harmonic distortion, in steady state condition and with different load current values. In this way, the proper functioning of the PWPC proposed in steady state is shown. Increased in step from 150 mA to 200 mA is shown in Fig. 10. Note that the duration of the transient is 40 ms and the voltage drop of v_1 and v_2 is around 10 V.

3.2 Test results in transient state

Likewise, when I_o is decreased in step from 200 mA to 150 mA is shown in Fig. 11. Note that the duration of the transient is 48.5 ms and the voltage overshoot of v_1 and v_2 is around 10 V. On the other hand, the transient response when vg is increased in step from 120V to 140 V, is shown in Fig. 12. We can see that the duration of the transient is 50 ms and the voltage overshoot of v_1 and v_2 is around 10 V.

Table 2 Performance comparison between the proposed method and other work.

	[5]	[17]	PWPC
Switching frequency (kHz)	50	10	50
Input voltage (V_{AC})	120	106	120
Power (W)	91	800	80
Power factor	0.99*	0.98*	0.9954
Total harmonic distortion	2.5*	3.1*	2
Duration of transient (ms)	500	300	50
Voltage drop (V)	25	10	10
Load change (%)	50-100	75-100	75-100

* Values obtained from hardware experimentation.

Similarly, the transient response when vg is reduced in step from 140 V to 120 V is shown in Fig. 13. Note that the transient period is 50 ms and the voltage drop of v_1 and v_2 is around 10 V. In addition, in Figs. 10-13, we can see that within the transient periods, the input current remains sinusoidal. We can also see that v_1 and v_2, are absolutely equal in the steady state and transient conditions, this confirms what was said in section 2, that the proposed control includes the scheme that was presented in [9], to eliminate the problem of voltage imbalance in capacitors.

Table 1 shows the performance comparison of the CPFCHBB parameters obtained in simulation, with the proposed control method and other works reported previously. Among these studies, is the one presented in [5], where the analysis is shown in detail CPFC-HBB, and the implementation of internal current loop with current averaging technique using a PID controller; the work presented in [17] is also included, where a simple analog control was proposed and implemented for the CPFC-HBB with the non-linear carrier control method.

Observing Table 2, the following can be stated: first, the power factor of the CPFC-HBB with the proposed PWPC is higher than power factors obtained in [5] [17]; second, the total harmonic distortion of the CPFC-HBB with the proposed PWPC is lower compared to [5] [17]; third; the transient response of CPFC-HBB with PWPC proposed is much faster than that presented in [5] [17]; finally, the voltage drop of the CPFC-HBB capacitors with the proposed PWPC is the same as in [17] and lower than in [5].

4. Conclusions

In this paper we presented a control technique for the prediction of the pulse width applied to an AC-DC converter with power factor correction, in half bridge boost topology.

The results show a power factor of 0.9954, transient response times to load change from 75% to 100% and *THD* of 2%, which are comparable with values reported in literature using techniques based on classic control laws. This implies that the proposed technique can achieve satisfactory results without revising performance parameters, or perform stability analysis.

It is also noteworthy that the algorithm proposed for the duty cycle prediction was obtained from the variables of state and average input, since it was based on the ACM. This implies an advantage over the techniques reported in literature that use instantaneous values of these variables, making measurement more difficult.

In future work, the converter will be implemented in hardware with the proposed control technique, verifying the results experimentally and comparing the resulting power factor with other existing techniques. In addition, the algorithm will be implemented to other topologies of AC-DC converters with power factor correction

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